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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,013	07/29/2002	Tajinder Manku	085907-000000US	5890

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EXAMINER	
JACKSON, BLANE J	
ART UNIT	**PAPER NUMBER**
2685	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,013	MANKU ET AL.	
	Examiner	Art Unit	
	Blane J Jackson	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-24,26,27,29,31 and 32* is/are rejected.

7)☒ Claim(s) *5-11 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7, 8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 12-24, 26-29, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ward et al. (U.S. Patent 4,736,390) with a view to Tilley et al. (U.S. Patent 6,225,848).

As to claims 1, 4 and 31, Ward teaches a radio frequency *down-converter* and method for reduced local oscillator leakage for demodulating an input signal X(t) comprising:

A synthesizer for generating mixing signals S1 and S2, which vary irregularly over time where S1 x S2 has significant power at the frequency of a local oscillator signal being emulated and neither S1 nor S2 has significant power at the frequency of the local oscillator signal being emulated (figure 2, S1 is PN code modulated LO and S2 is the PN code making them irregular in time, column 6, lines 45-60),

A first mixer coupled to the synthesizer for mixing the input signal X(t) with the mixing signal S1 to generate an output signal X(t)S1 (figure 2, mixer (30) or figure 4 for quadrature mixer configuration where the first mixer(s) are (44) and (47)), and,

A second mixer coupled to the synthesizer and to the output of the first mixer for mixing the signal X(t)S1 with the mixing signal S2 to generate an output signal X(t)S1S2 (figure 2, first mixer (30) and second mixer (34), column 5, lines 12 to column 6, line 10).

Ward teaches a technique for reducing the DC offset as regards to a zero or direct conversion IF receiver where DC offset is primarily due to RF leakage between the RF and oscillator ports of the mixer causing either the RF or local oscillator signal to mix with itself (column 4, line 63 to column 5, line 14). Ward does not teach this technique is applied to an up-converter.

Tilley teaches a closed loop error correction circuit for correcting DC offset applicable to analog and digital radio receivers and transmitters (figures 1-4, column 6, lines 42-60) where his technique is shown in the context of a radio receiver (column 5, lines 46). Tilley points out that even small quantities of DC offsets can saturate the signal path (column 1, lines 26-51). Since Tilley teaches the need for DC offset correction in the radio receiver and transmitter (column 5, lines 47-51), it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the DC offset reduction technique of Ward to the transmitter as well as the receiver as taught by Tilley to reduce the problems associated with DC offset in both sides of a transceiver.

As to claims 2 and 3, Ward teaches the synthesizer further comprises:

a synthesizer for generating mixing signals S1 and S2 where S1XS1XS2 or S1xS1xS2 does not have a significant amount of power within the bandwidth of the input signal X(t) at base band (figures 2 and 3A-3E, power removed by HPF after first mixer (30)).

As to claim 12, with respect to claim 3, Ward teaches the synthesizer for generating mixing signals S1 and S2 where the mixing signals S1 and S2 can change with time in order to reduce errors (the PN code modulated into the RF frequency and provided to the second mixer changes with time to reduce error, column 5, lines 12-23).

As to claims 13-17, Tilley of Ward modified teaches the details of a radio frequency up-converter of claim 3 further comprising a DC offset correction circuit comprising:

a DC offset generating circuit for generating a DC offset voltage (figure 2),

a summer for adding the DC offset voltage to an output of one of the mixers (summer (224)), and

a DC error level utilizing a power, voltage and current aspects of a measurement circuit for modifying the level of the DC offset voltage to minimize error level (closed loop of figure 2, column 2, lines 31-51, figure 3, column 3, line 67 to column 4, line 35).

As to claims 18 and 19, Ward teaches a filter for removing unwanted signal components for the X(t)S1 signal (figures 2 or 4, a low/ high pass filter (35), (36) or (45), column 5, lines 56-66).

As to claims 20-21, Ward teaches the mixing signals S1 and S2 are based on a pseudo-random noise generator (figure 2: PN Code Generator (33), column 5, lines 19-23 and column 7, lines 2-11).

As to claim 22, Ward teaches a synthesizer uses a single time base to generate both mixing signals S1 and S2 (PN code generator, considered part of the "synthesizer" drives both LO signal paths, figure 2).

As to claims 23 and 24, Ward teaches double balanced mixers with inherent port isolation since port isolation is necessary to reduce DC offsets (column 4, line 63 to column 5, line 4). It is well known in the art that Gilbert cell mixers require the local oscillator input to be a digital or square differential waveform to properly switch the modulating transistors on and off for expected performance.

As to claims 26 and 27 with respect to claim 4, Tilley of Ward modified teaches the closed loop error correction circuit comprises analogue components (column 6, lines 42-67) but is silent as to comprising a digital signal processor. Since Tilley also teaches providing the circuit as an IC with digital storage, it would have been obvious to one of

ordinary skill in the art at the time of the invention to alternatively employ a DSP in the circuit of Tilley of Ward modified to digitally process the DC offset error control loop.

As to claim 32, Ward (and Tilley) of Ward modified teaches an integrated circuit comprising the radio frequency up-converter of claim 1 (column 4, lines 43-49).

3. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ward et al. and Tilley et al. with a view to Bartusiak (U.S. Patent 6,016,422).

As to claim 25, Ward and Tilley do not teach a direct conversion transceiver where a local oscillator coupled to the synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of the local oscillator signal being emulated.

Bartusiak teaches a simple prior art method for generating radio frequency quadrature LO signals for direct conversion transceivers where the RF VCO runs at twice the frequency of the transmit signal frequency and applied to a signal generator system to both divide the frequency of the RF signal in half and generate a pair of signals in phase quadrature (figures 1-3, column 3, lines 7-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ward modified with the LO signal generation method of Bartusiak to obviate the need for an offset loop and to reduce the susceptibility of the RF VCO to remodulation.

Allowable Subject Matter

4. Claims 5-11 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Grandfield (U.S. Patent 5,448,772) discloses a stacked double balanced mixer circuit based on the Gilbert Cell. Pace et al. (U.S. Patent 5,471,665) discloses a differential DC offset compensation circuit for a direct conversion receiver.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJJ

NICK CORSARO
PRIMARY EXAMINER